WHAT IS CLAIMED IS:

1. A hierarchical processing apparatus comprising:

data input means for time-sequentially inputting pattern data in a particular hierarchical level;

a calculation parameter control data memory for storing calculation parameter control data;

detection means for detecting a particular feature from pattern data, using the calculation parameter control data;

an intermediate result memory for storing intermediate data output from the detection means; and

control means for controlling a flow of data depending on the hierarchical level of processing such that an input acquired via the data input means or an intermediate result fed back from the intermediate result memory and calculation parameter control data read from the calculation parameter control data memory are supplied to the detection means.

2. A hierarchical processing apparatus according to claim 1, wherein the detection means outputs an analog signal, and the intermediate result memory is a volatile analog memory.

3. A hierarchical processing apparatus according to claim 1, wherein the detection means outputs an analog

signal, and the intermediate result memory is a nonvolatile analog memory.

4. A hierarchical processing apparatus according to claim 1, further comprising calculation parameter change means for time-sequentially changing the calculation parameter.

5. A hierarchical processing apparatus according to claim 1, wherein the detection means extracts a particular local feature at respective locations in the data.

6. A hierarchical processing apparatus according to claim 1, wherein the detection means is parallel processing means including a plurality of operation elements disposed in parallel and coupled with each other.

7. A hierarchical processing apparatus according to claim 1, wherein the intermediate result memory includes a ferroelectric.

8. A hierarchical processing apparatus according to claim 1, further comprising conversion means for converting a signal output from the detection means into a digital signal, wherein the intermediate result memory is a digital

memory for storing the digital signal.

9. A hierarchical processing apparatus according to claim 8, wherein the digital memory is a ferroelectric memory.

10. A hierarchical processing apparatus according to claim 1, wherein the control means controls the flow of data such that the input acquired via the data input means or the intermediate result read from the intermediate result memory and calculation parameter control data read from the calculation parameter control data memory are supplied to the detection means with the same timing.

11. A hierarchical processing apparatus according to claim 1, wherein the detection means includes a plurality of sets of a feature detection layer and a feature consolidation layer that are cascade-connected.

12. A hierarchical processing apparatus according to claim 1, wherein the control means reads the calculation control data from the calculation parameter control data memory and controls calculation parameters of the detection means in accordance with the calculation control data so that features corresponding to a plurality of different

categories or sizes are detected from the input pattern data.

13. A hierarchical processing apparatus comprising:

data input means for inputting local data by scanning
pattern data in a particular hierarchical level;

first detection means for detecting a local feature
from the pattern data;

scanning position change means for changing a scanning
position of the data input means in accordance with the
class of the local feature;

second detection means for detecting, from a plurality
of local features detected at different scanning positions,
the presence/absence of a feature of a higher order than the
order of the detected local features;

an intermediate result memory for temporarily storing
data output from the second detection means; and

coupling means for feeding back a signal output from
the intermediate result memory to the first detection means.

14. A signal processor comprising:

a processing circuit;

circuit configuration information storage means for
storing circuit configuration information; and

circuit configuration control means for outputting a
control signal to the processing circuit in accordance with

the circuit configuration information read from the circuit configuration information storage means;

wherein the processing circuit comprises

a plurality of analog processing blocks for modulating an input signal;

a plurality of intermediate result memory blocks for temporarily storing signals output from the plurality of analog processing blocks;

a plurality of calculation parameter control data memory blocks for storing data used to control calculation parameters associated with the plurality of analog processing blocks; and

a plurality of signal lines for connections among the plurality of intermediate result memory block and/or the plurality of analog processing blocks;

whereby the circuit configuration control means controls reading of data from the calculation parameter control data memory block such that the processing circuit performs signal processing differently depending on the data read from the calculation parameter control data memory block.

15. A signal processor according to claim 14, wherein each analog processing block includes modulation means for modulating an input signal and a branch circuit for

outputting a signal via a selected output terminal.

16. A signal processor according to claim 14, wherein each analog processing block determines the sum or the integral of input signals weighted by factors varying with time.

17. A signal processor according to claim 14, wherein each analog processing block includes a plurality of modulators for modulating input signals by amounts that can be different from each other.

18. A signal processor according to claim 17, wherein each input signal modulator is a circuit for modulating the delay or phase of a pulse signal.

19. A signal processor comprising:

a processing circuit;

circuit configuration information storage means for storing circuit configuration information associated with the processing circuit and also storing data used to control the calculation parameter thereof;

circuit configuration control means for outputting a control signal to the processing circuit in accordance with the circuit configuration information and the calculation

parameter control data read from the circuit configuration information storage means;

wherein the processing circuit includes a plurality of switch blocks, a plurality of first-type analog processing blocks, a plurality of second-type analog processing blocks, and an intermediate result memory block for storing outputs of the second-type analog processing blocks, those blocks being connected with each other via signal lines with a particular connection pattern;

each first-type analog processing block modulates a signal output from a second-type analog processing block;

each second-type analog processing block consolidates signals input from a plurality of first-type analog processing blocks and outputs a resultant signal;

each switch block includes a plurality of switch elements and a plurality of signal lines; and

the circuit configuration control means controls the on/off-state pattern of the plurality of switch elements or controls the signal modulation parameters associated with the analog processing blocks such that the processing circuit performs signal processing differently depending on the on/off-state pattern or the signal modulation parameters.

20. A signal processor according to claim 19, wherein each switch block receives signals output from a plurality

of analog processing blocks via signal lines.

21. A signal processor according to claim 19, wherein each switch block includes a plurality of input/output signal lines and a plurality of switch elements, and each switch block transfers a signal input via a signal line to another signal line.

22. A signal processor according to claim 19, wherein each switch block sets the plurality of switch elements into an on-state or an off-state in accordance with a control signal supplied via a control line.

23. A signal processor according to claim 19, wherein each switch block includes a plurality of signal lines extending in the same direction.

24. A signal processor according to claim 19, wherein each of the first-type analog processing blocks includes modulation means for modulating an input signal, and each of the second-type analog processing blocks performs weighted integration on input signals with respect time.

25. A signal processor comprising:
a processing circuit;

circuit configuration information storage means for storing circuit configuration information and calculation parameter control data; and

circuit configuration control means for outputting a control signal to the processing circuit in accordance with the circuit configuration information and the calculation parameter control data read from the circuit configuration information storage means;

wherein the processing circuit includes a plurality of switch blocks each including a plurality of switch elements and a plurality of signal lines, a plurality of logical processing blocks, a plurality of analog processing blocks for modulating a signal input thereto, a plurality of intermediate result memory blocks for storing one or more signals output from some of the plurality of logical processing blocks or analog processing blocks, those blocks being connected with each other via signal lines; and

the circuit configuration control means controls the on/off-state pattern of the plurality of switch elements or controls the amounts of modulation performed by the analog processing blocks such that the processing circuit performs signal processing differently depending on the on/off-state pattern or the amounts of modulation.

26. A signal processor according to claim 25, wherein

each logical processing block includes at least one AND circuit having a plurality of inputs.

27. A pattern recognition apparatus comprising:

input means for inputting pattern data;

a processing circuit;

circuit configuration information storage means for storing circuit configuration information; and

circuit configuration control means for outputting a control signal to the processing circuit in accordance with the circuit configuration information read from the circuit configuration information storage means;

wherein the processing circuit includes at least a plurality of switches, a plurality of analog processing blocks, a plurality of intermediate result memory blocks for storing data output from some of the analog processing blocks, and signal lines for connections among the switches and/or analog processing blocks;

the circuit configuration information storage means stores at least one on/off-state pattern of the plurality of switches and one set of signal modulation data associated with the plurality of analog processing blocks; and

the circuit configuration control means includes output means that controls the on/off-state pattern of the plurality of switches and supplies particular calculation

parameter control data to the plurality of analog processing blocks in accordance with the circuit configuration information read from the circuit configuration information storage means such that a plurality of particular feature categories are detected at a plurality of particular locations from a part or all of the input pattern and the detected feature categories are output.